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|---|---|
| DARE, RYAN A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/759,483 | HOOKER, RODNEY E. | |
| | Examiner | Art Unit | |
| | Ryan Dare | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/04,12/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS: 12/12/05, 1/23/06*.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: Paragraph 11, lines 3-4 recite "first-in-first-out (LIFO)." This is repugnant to the common meaning in the memory art of LIFO as a last-in-first-out memory. The Examiner believes Applicant intended to recite "last-in-first-out (LIFO)" and has treated this as such for the remainder of this Office Action. This change is consistent with the rest of the specification.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 19 recites "a second number of clock cycles." A "second number of clock cycles" was already claimed in claim 10. The Examiner believes Applicant intended to limit claim 10 to the case where the already recited

second number of clock cycles is based on a physical address compare. By changing claim 19 to recite "said second number of clock cycles", the rejection under 35 U.S.C. 112 would be traversed.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 7-12, 16, 20, 23-29, and 32-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch, US Patent 5,930,820.

7. With respect to claim 1, Lynch teaches a variable latency cache memory, comprising:

an input, for specifying a type of an instruction requesting to read data from the cache memory, wherein said type is one of a plurality of predetermined instruction types, in col. 6, lines 56-60;

a plurality of storage elements, coupled to said input, for providing said data in a first number of clock cycles if said input specifies a first predetermined one of said plurality of predetermined instruction types, and for providing said data in a second number of clock cycles if said input specifies a second predetermined of said plurality of predetermined instruction types, wherein said first and second number of clock cycles is different, in col. 6, lines 26-39. The first predetermined type of Lynch corresponds to

the case in which data is stored in the top of the cache. The second predetermined type of instruction occurs when the data is not in the top of the cache, which takes more clock cycles.

8. With respect to claim 2, Lynch teaches the cache memory of claim 1, wherein said plurality of storage elements is configured as a last-in-first-out (LIFO) memory, in col. 2, lines 19-22.

9. With respect to claim 3, Lynch teaches the cache memory of claim 1, further comprising:

a second plurality of storage elements, coupled to said first plurality of storage elements, for caching non-stack data, whereas said first plurality of storage elements is for caching stack data, in col. 3, lines 18-21.

10. With respect to claim 7, Lynch teaches the cache memory of claim 1, wherein said first predetermined one of said plurality of predetermined instruction types comprises a pop instruction type, wherein said second predetermined one of said plurality of predetermined instruction types comprises a load instruction type, in col. 3, lines 45-46 and col. 4, lines 46-52. (An access to retrieve data in a conventional data cache is a load instruction)

11. With respect to claim 8, Lynch teaches the cache memory of claim 1, wherein a computer data signal embodied in a transmission medium comprising computer-readable program code provides the cache memory, in col. 4, lines 17-22.

12. With respect to claim 9, Lynch teaches the cache memory of claim 1, a computer program product comprising a computer usable medium having computer readable

program code causes the cache memory, wherein said computer program product is for use with a computing device, in col. 4, lines 17-22.

13. With respect to claim 10, Lynch teaches a variable latency cache memory, comprising:

a plurality of storage elements, configured as a last-in-first-out (LIFO) memory, having first and second subsets of said plurality of storage elements, said first subset for caching stack data more recently pushed than data cached in said second subset, in col. 3, lines 18- 25.

an input, for specifying an address of source data requested from the cache memory, in fig. 3, Address 64.

at least one comparator, coupled to said input, for comparing said address with one or more addresses of said data cached in said first subset of storage elements, wherein if said address hits in said first subset based on said comparing, the cache memory provides said source data from said first subset in a first number of clock cycles, wherein if said address does not hit in said first subset based on said comparing, the cache memory provides said source data in a second number of clock cycles, wherein said first and second number of cycles is different, in col. 6, lines 23-29.

14. With respect to claim 11, Lynch teaches the cache memory of claim 10, wherein if said address does not hit in said first subset based on said comparing, the cache memory provides said source data in a second number of clock cycles from said second subset if said address hits in said second subset, in col. 6, lines 23-29.

15. With respect to claim 12, Lynch teaches the cache memory of claim 10, wherein said address comprises a virtual address, in col. 1, line 62 through col. 2, line 12. A tag address is a virtual representation of the actual physical address.

16. With respect to claim 16, Lynch teaches the cache memory of claim 10, further comprising:

a second plurality of storage elements coupled to said first plurality of storage elements, for caching non-stack data, in col. 3, line 24, "cache storage."

17. With respect to claim 20, Lynch teaches the cache memory of claim 10, wherein said first subset comprises a top one of said plurality of storage elements, in col. 9, lines 52-56. When a standard pop command is performed, the top one of the storage elements is accessed.

18. With respect to claim 23, Lynch teaches the cache memory of claim 10, wherein said address comprises a source address of a load instruction, in col. 1, line 62 through col. 2, line 4.

19. With respect to claim 24, Lynch teaches the cache memory of claim 19, wherein a computer data signal embodied in a transmission medium comprising computer-readable program code provides the cache memory, in col. 4, lines 17-22.

20. With respect to claim 25, Lynch teaches the cache memory of claim 10, a computer program product comprising a computer usable medium having computer readable program code causes the cache memory, wherein said computer program product is for use with a computing device, in col. 4, lines 17-22.

21. With respect to claim 26, Lynch teaches a method for providing data from a cache memory with a variable latency, the method comprising:

storing stack data into the cache memory in a last-in-first-out manner, in col. 2, lines 19-22;

providing load data from the cache memory in a first number of clock cycles if a virtual address of the load data hits in the cache memory, in col. 6, lines 36-39.

providing the load data from the cache memory in a second number of clock cycles if the virtual address of the load data misses in the cache memory but a physical address of the load data hits in the cache memory, wherein the first and second number of clock cycles is different, in col. 6, lines 23-39.

22. With respect to claim 27, Lynch teaches the method of claim 26, further comprising:

determining whether the virtual address hits in a top subset of cache lines of the cache memory, wherein the top subset is less than all cache lines of the cache memory, in col. 6, lines 26-28.

23. With respect to claim 28, Lynch teaches the method of claim 27, wherein the top subset of cache lines of the cache memory comprises cache lines implicated by the most recently pushed stack data, in col. 6, lines 26-28 and col. 2, lines 22-24.

24. With respect to claim 29, Lynch teaches the method of claim 26, wherein the first number of clock cycles is less than the second number of clock cycles, in col. 4, lines 46-52.

25. With respect to claim 32, Lynch teaches a method for providing data from a cache memory with a variable latency, the method comprising:

determining whether a request for data from the cache memory is in response to a pop or load instruction, in col. 6, lines 26-34;

providing the data in a first number of clock cycles if the request is in response to a pop instruction, in col. 4, lines 46-52, as well as in col. 6, lines 36-39 and col. 11, lines 34-39;

providing the data in a second number of clock cycles if the request is in response to a load instruction, wherein the first and second number of clock cycles is different, in col. 46, lines 46-48. It is disclosed in the sections of the reference listed above that this conventional load instruction takes more clock cycles than the stack pop instruction.

26. With respect to claim 33, Lynch teaches the method of claim 32, wherein the first number of clock cycles is less than the second number of clock cycles, in col. 4, lines 46-52.

27. With respect to claim 34, Lynch teaches the method of claim 32, wherein said providing the data in the first number of clock cycles if the request is in response to a pop instruction is speculative subject to a subsequent determination that a source address of the data hits in the cache memory, in col. 2, lines 56-61.

28. With respect to claim 35, Lynch teaches the method of claim 32, wherein a load instruction comprises an instruction explicitly specifying a source address of the data, in col. 1, line 62 through col. 2, line 12.

29. With respect to claim 36, Lynch teaches the method of claim 32, wherein a pop instruction comprises an instruction inherently specifying a source address of the data, in col. 4, lines 46-47.

30. With respect to claim 37, Lynch teaches the method of claim 36, wherein the pop instruction inherently specifies the source address of the data relative to a stack pointer value, in col. 6, lines 6-13.

31. With respect to claim 38, Applicant claims a computer data signal embodied in a transmission medium comprising computer-readable program code for providing the variable latency cache memory of claim 1, and is therefore rejected using similar logic.

32. With respect to claim 39, Applicant claims a computer data signal embodied in a transmission comprising computer-readable program code for providing the variable latency cache memory of claim 10, and is therefore rejected using similar logic.

### *Claim Rejections - 35 USC § 103*

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

35. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1-3, 7-12, 16, 20, 23-29, and 32-39 above, in view of Healey, US Patent 3,810,117.

36. With respect to claim 21, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that the offset in the cache memory which controls the size of the first plurality of storage elements can be precisely two. Healey teaches separating the first X number of entries from the top of the stack in order to have faster access to them, in col. 1, lines 24-39. It is disclosed that the top two entries in the stack can form a subset in col. 1, lines 46-54, thereby teaching:

The cache memory of claim 10, said first subset comprises a top two of said plurality of storage elements.

37. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the stack cache storage system of Lynch with the stack cache storage system of Healey in order to have a small subset of stack elements that are quicker and easier to access than the rest of the storage, as taught by Healey in col. 1, lines 17-23.

38. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1-3, 7-12, 16, 20, 23-29, and 32-39 above, in view of Tremblay et al., US Patent 6,038,643.

39. With respect to claim 22, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that the offset in the cache memory which controls the size of the first plurality of storage elements can be precisely three. The Healey reference used above for claim 22 teaches separating the first X number of entries from the top of the stack in order to have faster access to them. The Healey reference also fails to expressly disclose that the number of items can be three. Tremblay et al. resolves this deficiency in the prior art by keeping the top three elements of the stack in a separate, faster storage area in col. 18, lines 51-58, thereby teaching the limitation:

The cache memory of claim 10, wherein said first subset comprises a top three of said plurality of storage elements.

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stack cache storage system of Lynch with the stack cache storage system of Healey in order to have a small subset of stack elements that are quicker and easier to access than the rest of the storage, as taught both by Healey in col. 1, lines 17-23, as well as by Tremblay et al., in col. 18, lines 51-55.

41. Claims 4-6, 17-19, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1-3, 7-12, 16, 20, 23-29, and 32-39 above, in view of Sager et al., US Patent 6,425,055.

42. With respect to claim 4, Lynch teaches all other limitations of the parent claim but discloses that the second and third number of clock cycles are substantially equal (col.

2, lines 63-67). Sager et al. resolves this deficiency, having 3 separate times for the three cases of: 1) virtual address hit, 2) physical address hit, and 3) true hit/miss. See col. 18, lines 18-25. It is disclosed therein that several clock cycles elapse between determination of the virtual address and physical address computation. Only after it is determined that the physical address is not in the cache, a miss is signaled, which indicates that another portion of memory must be referenced for the data. Therefore Sager et al. teaches the claim:

The method of claim 26, further comprising:

the cache memory of claim 3, wherein said second plurality of storage elements provides said data in a third number of clock cycles if said input specifies said second predetermined one of said plurality of predetermined instruction types, wherein said second and third number of clock cycles is different.

43. It would have been obvious to one of ordinary skill in the art at the time the invention was made, having the teachings of Lynch and Sager et al. before him to modify the cache memory system of Lynch with the cache memory system of Sager et al. because speculatively determining a cache line allows you to use it before a physical address is computed, thus saving clock cycles, as taught by Sager et al. in col. 2, lines 11-14.

44. With respect to claim 5, the combination of Lynch and Sager et al. teach all other limitations of the parent claims as discussed supra. Sager et al. further teach the cache memory of claim 4, wherein said third number of clock cycles is greater than said

second number of clock cycles, in col. 18, lines 25. Also see the above discussion of claim 4.

45. With respect to claim 6, the combination of Lynch and Sager et al. teach all other limitations of the parent claims as discussed supra. Lynch et al. further teaches the cache memory of claim 5, wherein said second predetermined one of said plurality of predetermined instruction types comprises a load instruction type, in col. 6, lines 23-39.

46. With respect to claim 17, Lynch teaches all other limitations of the parent claims, but discloses that the second and third number of clock cycles are substantially equal (col. 2, lines 63-67). Sager et al. resolves this deficiency, having 3 separate times for the three cases of: 1) virtual address hit, 2) physical address hit, and 3) true hit/miss. See col. 18, lines 18-25. It is disclosed therein that several clock cycles elapse between determination of the virtual address and physical address computation. Only after it is determined that the physical address is not in the cache, a miss is signaled, which indicates that another portion of memory must be referenced for the data. Therefore Sager et al. teaches the claim:

The cache memory of claim 16, wherein said second plurality of storage elements provides said data in a third number of clock cycles if said address does not hit in said first plurality of storage elements, wherein said second and third number of clock cycles is different.

47. It would have been obvious to one of ordinary skill in the art at the time the invention was made, having the teachings of Lynch and Sager et al. before him to modify the cache memory system of Lynch with the cache memory system of Sager et

al. because speculatively determining a cache line allows you to use it before a physical address is computed, thus saving clock cycles, as taught by Sager et al. in col. 2, lines 11-14.

48. With respect to claim 18, the combination of Lynch and Sager et al. teach all other limitations of the parent claims as discussed supra. Sager et al. further teach the cache memory of claim 17, wherein said third number of clock cycles is greater than said second number of clock cycles, in col. 18, lines 25. Also see the above discussion of claim 17.

49. With respect to claim 19, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that the second number of clock cycles is based on a physical address compare. Sager et al. teach the cache memory of claim 10, wherein if said address does not in said first subset based on said comparing, the cache memory provides said source data in a second number of clock cycles based on a physical address compare, in col. 5, lines 11-25.

50. With respect to claim 30, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that loaded data is speculative subject to determination of a physical address. Sager et al. teaches a method wherein providing the load data from the cache memory in the first number of clock cycles if the virtual address of the load data hits in the cache memory is speculative subject to a subsequent determination that the physical address of the load data hits in the cache memory, in col. 5, lines 11-25.

51. With respect to claim 31, Lynch teaches all other limitations of the parent claims, but discloses that the first and third number of clock cycles are substantially equal (col. 2, lines 63-67). Sager et al. resolves this deficiency, having 3 separate times for the three cases of: 1) virtual address hit, 2) physical address hit, and 3) true hit/miss. See col. 18, lines 18-25. It is disclosed therein that several clock cycles elapse between determination of the virtual address and physical address computation. Only after it is determined that the physical address is not in the cache, a miss is signaled, which indicates that another portion of memory must be referenced for the data. Therefore Sager et al. teaches the claim:

The method of claim 26, further comprising:

providing the load data from a non-stack cache memory in a third number of clock cycles if the virtual address and the physical address miss in the cache memory, wherein the first and third number of clock cycles is different.

***Conclusion***

52. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar cache memory storage systems.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
March 3, 2006

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